AMENDMENTS TO THE DRAWINGS

The attached four replacement sheets of drawings include changes to Figures 1A through 1G.

The replacement sheet which includes Figures 1A and 1B, replaces the original sheet including figures 1A and 1B. In both Figures 1A and 1B, previously omitted label -- Prior Art -- has been added.

The replacement sheet which includes Figures 1C and 1D replaces the original sheet including Figures 1C and 1D. In both Figures 1C and 1D, previously omitted label -- Prior Art -- has been added.

The replacement sheet which includes Figures 1E and 1F replaces the original sheet including Figures 1E and 1F. In both Figures 1E and 1F, previously omitted label -- Prior Art -- has been added.

The replacement sheet which includes Figure 1G replaces the original sheet including Figure 1G. In Figure 1G, previously omitted label -- Prior Art -- has been added.

Attachment: Four replacement sheets.

REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Official Action dated 7 June 2005. Responsive to the objection and rejections applied to the claims of the subject Patent Application, Claim 1 has been amended to further clarify the combination of elements that defines the invention of the subject Patent Application.

In the Official Action, Figures 1A through 1G of the drawings were objected as failing to be designated by a legend such as -- Prior Art --. In order to avoid abandonment of the Application, the corrected drawings of Figures 1A through 1G on four replacement sheets, designated by a label such as -- Prior Art -- have been submitted in the Appendix following page 13 of this paper in compliance with 37 CFR 1.121(d).

In the Official Action, Claim 1 was objected to because of found informalities. Accordingly, Claim 1 has been amended to designate a first shallow layer as being of a "second conductivity type" and a second shallow layer as being of "a conductivity type opposite to said second conductivity type of said first shallow layer". It is believed, that by this amendment, the objection of Claim 1 has been overcome; and the same is respectfully requested.

Further, in the Official Action, Claims 1, 2, 6 – 8, 10 and 12 were rejected under 35 U.S.C. § 102(e) as being anticipated by Takano et al., U.S. Patent 6,717,210; Claims 3, 4 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Takano et al. in view of Letavic, U.S. Patent 6,551,881; and

Claim 11 (mistakenly mentioned by the Examiner as Claim 12) was rejected under 35 U.S.C. § 103(a) as being unpatentable over Takano et al. in view of Williams et al., U.S. Publication 2005/0035398.

Prior to discussion of the differences between the cited prior art and the subject invention as presented in the current Patent Application, it is believed that a brief review of the cited prior art is in order.

Takano et al., a main reference cited by the Examiner, is directed to a trench gate type semiconductor device and fabricating method of the same. The fabrication process of the MOS transistor 100 includes the following steps: N- type layer 2 is grown on a principle surface of the N+ type silicone substrate 1. Then, by means of ion implantation, a chosen P type impurity is doped into the surface of the layer 2. The doped impurity further is thermally diffused to form a P type base layer 3. Further, as shown in Figure 4, implant ions of an N type impurity are implanted into the surface of the P base layer 3 at a high concentration. Then, the dopant is thermally diffused thereby forming an N+ type source layer 4.

Next, as shown in Figures 5 and 6, trench 5 is formed for the gate electrode 7. The gate electrode is formed through the source layer 4, base layer 3 and epitaxial layer 2. The poly-silicone layer 71 fills the trench 5 and extends over the source layer 4. Thereafter, as shown in Figure 9, a film 103 is deposited and rapid thermal anneal technique to thermally process the resultant device structure is performed. Subsequently, contact openings 104 in the film 8 are defined in the

source regions each of which is laterally interposed between adjacent gate electrode 7. At the bottom of each contact hole 104, a groove 9 is formed which penetrates the source layer 4 and reaches its underlying P base layer 3 as shown in Figure 12. This groove 9 has its bottom portion at which the P base layer 3 is partially exposed. A P+ type diffusion layer 10 is formed at the exposed portion of P base 3. Lastly, as shown in Figure 2, a source electrode 11 and a drain electrode 12 are formed on the top and bottom surfaces of the resultant structure.

It is respectfully submitted, that Takano et al. reference fails to suggest, disclose or render obvious the method which the Applicant regards as the invention and which is clearly covered by Claim 1, as amended. Specifically, in the manufacturing process of Takano et al., as shown in Figures 4 – 6 the source N+ layer 4 is formed on the surface of the P base layer 3 prior to formation of the gate contacts (column 4, line 46 – column 5, line 25).

While in the present invention, a source N+ doped region 42 (a first shallow layer) is formed on the base region 38 after the gate 40 has been formed in the base region 38.

This difference between the present invention and Takano et al. is clearly emphasized in Claim 1, which now includes (inter alia) a following recitation:

"... forming at least one gate in said base region;

after formation of said at least one gate, heavily doping ... a first surface of said base region containing at least one gate formed therein for forming on said

base region and in juxtaposition to said at least one gate a first shallow layer of a second conductivity type ..."

This features is completely missing from Takano et al. Therefore, as Takano et al. fails to disclose each and every one of the claimed elements, it cannot anticipate the invention of the subject Patent Application, as now claimed. Accordingly, Claim 1, as amended, is believed to be allowable over Takano et al.; and the same is respectfully urged.

Letavic, another reference cited by the Examiner is directed to a self-aligned dual –oxide UMOSFET device and a method for fabricating the same. As shown in Figure 1, substrate 12 is provided which is etched to form trenches 20A and 20B. Then, a thick thermal oxide layer 30 is grown on the sidewalls and floor of each trench. Thereafter, a subsequent silicon nitride layer 40 is conformally deposited on to the thick oxide layer 30. Referring to Figure 2, the top silicon nitride layer 40 of the layer of the trench etched structure is implanted with boron using the multiple energy large angle tilt implant technique. The implantation of boron occurs over the top surfaces of the substrate mesas 14A, 14B and 14C. The angle tilt field allows boron to be implanted at predetermined depths in trenches 20A and 20B along the sidewalls 22 and 24.

As shown in Figure 5, the UMOSFET 100 further includes a drain 102 connected by metallization to the substrate 12. The source 104 is a N type source which includes a plurality of N+ doped islands 104A, 104A', 104B, 104B' and 104C, 104' implanted into the surface of the P channel by the doping regions 55A,

55B and 55C. The mask for this has a hole in it at the center of the substrate mesas 14A, 14B, 14C.

It is respectfully submitted, that in Letavic, in contrast to the present invention, an inclined ion implantation is used for forming a gate structure, whereas the source islands 104A, 104A', 104B, 104B' and 104C, 104C' are formed not by inclined ion implantation but through the mask, as described in column 6, line 34 – 40.

While in the present invention, the inclined ion implantation is used for formation of the N+ doped region 42 (source structure) of the semiconductor device of the present invention. The inclined ion implantation is performed after the gates have been formed.

Further, although Letavic describes the inclined ion implantation process, the reference however fails to describe a combined vertical and inclined ion implantation of a dopant.

While in the present invention, a first surface of the base region 38 is heavily doped by means of a combined vertical and inclined ion implantation of a dopant into a first surface of the base region containing gates formed therein.

Therefore, in contrast to the present invention, Letavic fails to suggest, disclose or render obvious a process of "... heavily doping by combined vertical and inclined ion implantation of a dopant into ... base region containing said at least one gate formed therein ...".

Williams et al., a reference cited by the Examiner, is directed to a trench MOSFET with recessed clamping diode which includes an epitaxal layer over a substrate of like conductivity and trenches containing thick bottom oxide, sidewall gate oxide, and conductive gates.

The process for fabrication the device of Williams et al., includes a 20 second rapid thermal anneal or a 10 minute 950 C thermal anneal which follow source implantation (paragraph 0169).

It is respectfully submitted, that in contrast to the present invention, Williams et al. fails to suggest, disclose or render obvious a heavy doping by combined vertical and inclined ion implantation of a dopant into a base region which contains at least one gate formed therein for forming on the base region and adjacent to the gate a first shallow layer. This step of forming a source structure is completely missing from Williams et al.

It is respectfully submitted, that none of the references cited by the Examiner, either taken singly or in combination thereof, suggests, discloses or render obvious the method for forming a semiconductor device which would include (inter alia) the following steps:

"forming at lest one gate in said base region;

after formation of said at least one gate, heavily doping by combined vertical and inclined ion implantation of a dopant into a first surface of said base region containing said at least one gate formed therein for forming on said base region and in juxtaposition with said at least one gate a first shallow layer ...".

This feature is clearly emphasized in Claim 1, as amended. Therefore, the allowability of Claim 1 is believed; and the same is respectfully requested.

Claims 4 – 12 directly or indirectly dependent upon Claim 1 are believed each to add further limitations that are patentably distinct in addition to being dependent upon what is now believed to be a patentable base claim, and therefore, allowable for at least the same reasons.

Claims 2 and 3 have been cancelled without prejudice to incorporate the subject matter thereof into Claim 1.

For all the foregoing reasons, it is now believed that the subject Patent Application has been placed in condition for allowance, and such action is respectfully requested.

Respectfully requested,
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Dated: 6 Dec. 2005

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